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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,642	09/29/2004	Oleg Gluschenkov	FIS920040196US1	5641
45094	7590	11/29/2005	EXAMINER	
HOFFMAN, WARNICK & D'ALESSANDRO LLC			LINDSAY JR, WALTER LEE	
75 STATE ST			ART UNIT	
14TH FL			PAPER NUMBER	
ALBANY, NY 12207			2812	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/711,642		GLUSCHENKOV ET AL.	
	Examiner		Art Unit	
	Walter L. Lindsay, Jr.		2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

This Office Action is in response to an Application filed on 9/22/2005.

Currently, claims 1-20 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Adetutu et al. (U.S. Patent No. 6,902,969 filed 7/31/2003).

Adetutu shows the method as claimed in Figs. 1-7 and corresponding text as: depositing a material (116) having a first work function (col. 2, lines 15-32); forming a conductive hard mask (118) including one of a metal containing conductor and a metal silicide over the material (col. 3, lines 7-18); using a photoresist mask (124, 126) to remove the conductive hard mask from an area for a device having a second, different work function selective to the material (col. 3, lines 33-53); and removing the photoresist mask, leaving the conductive hard mask for use in removing the material from the area and inclusion in the metal gate electrode (col. 3, lines 54-67) (claim 1). Adetutu teaches that the metal silicide includes one of tungsten silicide (WSi), titanium silicide (TiSi_x), tantalum silicide (TaSi_x), nickel silicide (NiSi), cobalt silicide (CoSi_x), and the metal

Art Unit: 2812

containing conductor includes one of tantalum nitride (TaN) and tantalum silicon nitride (TaSiN) (col. 3, lines 7-18) (claim 2). Adetutu teaches that the conductive hardmask has a thickness of no less than 10Å and no greater than 500Å (col. 3, lines 33-53) (claim 3). Adetutu teaches that the conductive hardmask has a thickness of no less than 20Å and no greater than 500Å (col. 3, lines 33-53) (claim 4). Adetutu teaches that the photoresist removing step includes conducting a wet etch using a chemistry including at least one of sulfuric acid (H₂SO₄) and peroxide (H₂O₂) (piranha etch) (col. 2, line 61-col. 3, line 6) (claim 5)

Adetutu shows the method as claimed in Figs. 1-7 and corresponding text as: forming a gate dielectric (114); depositing a material (116) having a first work function (col. 2, lines 15-32); depositing a conductive hard mask on the first metallic conductor (118) including one of a conductor and a metal silicide (col. 3, lines 7-18); removing the conductive hard mask from an area for a particular device type using a photoresist mask selective to the first metallic conductor (col. 3, lines 33-53); removing the photoresist mask (col. 3, lines 54-67); removing the first metallic conductor in the area with the conductive hard mask protecting the first metallic conductor (col. 3, lines 19-32); depositing a conductor (120); and forming the gate electrode (137) (col. 3, lines 54-67)(claim 6). Adetutu teaches that the conductor depositing step includes depositing a second metallic conductor having a different, second work function, and depositing a silicon-containing conductor (col. 3, lines 7-18) (claim 7). Adetutu teaches that the conductor depositing step includes depositing a silicon-containing conductor (col. 3, lines 7-18) (claim 8). Adetutu teaches that the first metallic conductor includes a p-type

Art Unit: 2812

metal, and the silicon-containing conductor is highly doped n-type (col. 4, lines 49-67) (claim 9). Adetutu teaches that the metal silicide includes one of tungsten silicide (WSi), titanium silicide (TiSi_x), tantalum silicide (TaSi_x), nickel silicide (NiSi), cobalt silicide (CoSi_x), and the metal containing conductor includes one of tantalum nitride (TaN) and tantalum silicon nitride (TaSiN) (col. 3, lines 7-18) (claim 10). Adetutu teaches that the conductive hardmask has a thickness of no less than 10Å and no greater than 500Å (col. 3, lines 33-53) (claim 11). Adetutu teaches that the conductive hardmask has a thickness of no less than 20Å and no greater than 500Å (col. 3, lines 33-53) (claim 12). Adetutu teaches that the conductive hard mask removing step includes conducting one of a wet etch and a reactive ion etch (dry etch) (col. 3, lines 19-32) (claim 13). Adetutu teaches that the photoresist removing step includes conducting a wet etch using a chemistry including at least one of sulfuric acid (H₂SO₄) and peroxide (H₂O₂) (piranha etch) (col. 2, line 61-col. 3, line 6) (claim 14). Adetutu teaches that the first metallic conductor removing step includes using the wet etch (col. 2, line 61-col. 3, line 6) (claim 15).

Adetutu shows the method as claimed in Figs. 1-7 and corresponding text as:

depositing a dielectric (114) on a substrate; depositing a material (116) having a first work function over the dielectric (col. 2, lines 15-32); depositing a conductive hard mask on the first metallic conductor (118) including one of a conductor and a metal silicide (col. 3, lines 7-18); removing the conductive hard mask from an area for a particular device type using a photoresist mask selective to the first metallic conductor (col. 3, lines 33-53); removing the photoresist mask (124) to a remaining portion of the

Art Unit: 2812

conductive hard mask (col. 3, lines 54-67) ; removing the first metallic conductor in the area with the conductive hard mask protecting the first metallic conductor (col. 3, lines 19-32); depositing a second metal (118) having a second, different work function in the area (col. 3, lines 7-18) depositing a silicon-containing conductor (120) over the first and second metals (col. 3, lines 7-18); and forming the metal gate electrode (137) (col. 3, lines 54-67)(claim 16). Adetutu teaches that the metal silicide includes one of tungsten silicide (WSi), titanium silicide (TiSi_x), tantalum silicide (TaSi_x), nickel silicide (NiSi), cobalt silicide (CoSi_x), and the metal containing conductor includes one of tantalum nitride (TaN) and tantalum silicon nitride (TaSiN) (col. 3, lines 7-18) (claim 17). Adetutu teaches that the conductive hardmask has a thickness of no less than 10Å and no greater than 500Å (col. 3, lines 33-53) (claim 18). Adetutu teaches that the conductive hardmask has a thickness of no less than 20Å and no greater than 500Å (col. 3, lines 33-53) (claim 19). Adetutu teaches that the conductive hard mask removing step includes conducting one of a wet etch and a reactive ion etch (dry etch) (col. 3, lines 19-32) (claim 20).

Response to Arguments

3. Applicant's arguments filed 9/22/2005 have been fully considered but they are not persuasive. The examiner views layer (118) as a mask layer because it is used during the etch process over (116) in the formation of gate (137). It is also the view of the examiner that the work function in the region including (116) is different from that of the region only having layer (118) remaining. The layer (118) is also removed from portions of the substrate.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2812

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL

November 23, 2003